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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,471	05/03/2001	Sukeyuki Shinotsuka	263/196	6954

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EXAMINER	
YAM, STEPHEN K	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/848,471	SHINOTSUKA ET AL.	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 14, 2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx et al. US Patent No. 5,933,190 (hereinafter Dierickx '190) in view of Dierickx US 2005/0167602 (hereinafter Dierickx '602) (parent application 09/460,473 filed December 14, 1999 contains the portions of the disclosure and the figures cited by Examiner for this rejection).

Regarding Claim 2, Dierickx '190 teaches (see Fig. 1, 2, 4) an image sensor comprising a number of light sensor circuits arranged to form a matrix of pixels (see Fig. 1), each of said circuits being capable of producing in a photoelectric converting element (10) a sensor current proportional to the quantity of light falling thereon (see Col. 4, lines 38-40) and converting the produced current into a voltage signal by using a MOS type transistor (11) with a logarithmic

output characteristic in a weak inverse state (see Col. 4, lines 42-45). Dierickx '190 does not teach a voltage switching-over circuit for changing a drain voltage of each of said MOS type transistors for each of said pixels to a value lower than a normal value for a specified time to remove a charge accumulated in a parasitic capacitance of the photoelectric element before detecting a light signal from each pixel. Dierickx '602 teaches (see Fig. 5) a similar device, with each pixel containing a photoelectric converting element (12), a MOS type transistor (11), and a voltage switching-over circuit (reference transistor) (see Paragraph 0060) for changing a drain voltage of each of said MOS type transistors (see Paragraph 0060) for each of said pixels to a value lower than a normal value for a specified time (see Fig. 6) to remove a charge accumulated in a parasitic capacitance of the photoelectric element (see Paragraph 0028) before detecting a light signal from each pixel (see Fig. 6 and Paragraph 0059). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the voltage switching-over circuit of Dierickx '602 in the image sensor of Dierickx '190, to provide improved signal accuracy and reduce residual charges on the photoelectric conversion element.

Regarding Claim 3, Dierickx '190 in view of Dierick '602 teach the elements in Claim 3, with Dierickx '190 further teaching a pixel-line selecting circuit (6) for successively selecting pixel lines, a pixel selecting circuit (14) for successively selecting pixels in one selecting line, both of said selecting circuits cooperating together to successively scan and read sensor signals from respective pixels in a time series (by multiplexing- see Col. 4, lines 7-19).

Regarding Claim 4, Dierickx '190 teach each of the light sensor circuit is composed of said MOS type transistor for converting a sensor current flowing in the photoelectric converting element to a voltage signal by using its logarithmic output characteristic in a weak inverse state

(see Col. 4, lines 40-45, 49-51), a second transistor (13) for amplifying the voltage signal (see Fig. 2 and Col. 4, lines 45-46) and a third transistor (14) for outputting a sensor signal corresponding to the amplified voltage signal at a specified moment of time (when activated by activating line 15).

Regarding Claim 5, Dierickx '190 in view of Dierick '602 teach the image sensor in Claim 3, according to the appropriate paragraph above. Dierickx '190 does not teach a sample-and-hold circuit provided on an output side of each pixel in each pixel line. It is well known in the art to utilize a sample-and-hold circuit in an image sensor system, to convert an analog image signal to a digital value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a sample-and-hold circuit on an output side of each pixel in each pixel line in the image sensor of Dierickx '190 in view of Dierickx '602, to convert the analog image signal to a digital signal for image processing and binary storage of the image signal.

Response to Arguments

4. Applicant's arguments with respect to claims 2-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SY

THANH X. LUU
PRIMARY EXAMINER